Attorney's Docket No.: 10559-364001/Intel P8247-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : David I. Poisner
Serial No.: 09/672,345
Filed : September 28, 2000
Title : ACCESSING MULTI-PORTED MEMORY

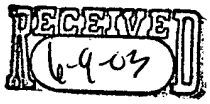
Art Unit: 2186
Examiner: Hong Chong Kim
Assignee: Intel Corporation

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DRAFT

RESPONSE

In response to the action mailed **April 8, 2003**, please amend the application as follows:



CERTIFICATE OF MAILING BY FIRST CLASS MAIL
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit

Signature

Typed or Printed Name of Person Signing Certificate

Date June 9, 2003

To Examiner Hong Kim

Telephone: (703) 305-3835

Facsimile number (703) 746-7240

From Linda G. Gunderson

Re P8247-2 METHOD AND APPARATUS USING DUAL-PORTED MEMORY FOR PERFORMANCE ENHANCEMENT
Your Ref.: 09/672,345
Our Ref.: 10559-364001

Number of pages including this page 16

Message Here is a draft response to the office action, so you can see what I'm thinking. I'd appreciate a call to discuss the Dinwiddie reference. My direct # is (858) 678-4311. Thanks--Linda

Attorney's Docket No.:10559-364001/
Intel P8247-2

In the claims:

In the claims:

DRAFT

1. (Previously Amended) A computer system, comprising:

a non-cached multi-ported memory;

a main memory;

a central processing unit coupled to the multi-ported memory;

a bus configured to communicate with one or more peripheral devices, the bus coupled to the multi-ported memory and configured to access the multi-ported memory independently of the central processing unit;

wherein the computer system is configured so that control accesses from the central processing unit are directed to the multi-ported memory and not to the main memory and data accesses from the central processing unit are directed to the main memory and not to the dual-ported memory.

2. (Original) The system of claim 1, further comprising an operating system executing on the central processing unit, wherein the operating system is configured such that accesses to the multi-ported memory are not cached.

DRAFT

3. (Original) The system of claim 1, wherein the multi-ported memory is dual-ported.

4. (Original) The system of claim 1, wherein the multi-ported memory is embedded within a memory controller.

5. (Original) The system of claim 4, wherein the multi-ported memory and memory controller are integrated into a single chip.

6. (Previously Amended) The system of claim 1, wherein the multi-ported memory is chosen from the group consisting of static random access memory and dynamic random access memory.

7. (Original) The system of claim 1, wherein the multi-ported memory stores reservation bits mapped to blocks of general-purpose memory in the multi-ported memory.

8. (Original) The system of claim 1, wherein virtual addresses within multi-ported memory are mapped to physical addresses with smart addressing.

DRAFT

9. (Original) The system of claim 1, wherein the coupling of the peripheral device to the memory controller includes an input/output bus.

10. (Previously Amended) A method comprising:

routing a data access from a peripheral device to a first memory in the computer and not to a second memory in the computer; and

routing a status access from a peripheral device to [a] the second memory in the computer and not to the first memory in the computer.

11. (Original) The method of claim 10, wherein the first memory comprises main memory.

12. (Original) The method of claim 10, wherein the second memory comprises memory included in a memory controller.

13. (Original) The method of claim 10, wherein the second memory is dual-ported.

14. (Previously Amended) An article comprising a computer-readable medium which stores computer-executable

DRAFT

instructions for memory accessing, the instructions causing a machine to:

route a data access from a peripheral device to a first memory in the computer and not to a second memory in the computer; and

route a status access from the peripheral device to [a] the second memory in the computer and not to the first memory.

15. (Original) The article of claim 14, wherein the computer includes an input/output controller.

16. (Original) The article of claim 14, wherein the first memory comprises main memory.

17. (Original) The article of claim 14, wherein the second memory comprises memory included in a memory controller.

18. (Previously Amended) The article of claim 14, wherein the second memory is dual-ported.

19. (Previously Amended) A method comprising:

DRAFT

routing the a data access from a central processing unit to a first memory in the computer and not to a second memory in the computer; and

routing a control access from the central processing unit to [a] the second memory in the computer and not to the first memory.

20. (Original) The method of claim 19, wherein the first memory comprises main memory.

21. (Previously Amended) The method of claim 19, wherein the second memory is included in a memory controller.

22. (Original) The method of claim 19, wherein the second memory is dual-ported.

23. (Previously Amended) An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

route a data access from a central processing unit to a first memory in the computer and not to a second memory in the computer; and

DRAFT

route a control access from the central processing unit to [a] the second memory in the computer and not to the first memory in the computer.

24. (Original) The article of claim 23, wherein the first memory comprises main memory.

25. (Original) The article of claim 23, wherein the second memory comprises memory included in a memory controller.

26. (Original) The article of claim 23, wherein the second memory is dual-ported.

27. (Previously Amended) An integrated circuit comprising:

a memory controller configured to communicate with a CPU, a peripheral device, and a main memory, the memory controller including a multi-ported memory, wherein the memory controller is to direct control accesses for the CPU [are directed] to the multi-ported memory and not to the main memory, and wherein the memory controller is to direct data accesses for the CPU [are directed] to the main memory and not to the multi-ported memory.

DRAFT

28. (Original) The integrated circuit of claim 27, wherein the multi-ported memory is dual-ported.

29. (Previously Amended) The integrated circuit of claim 27, wherein the multi-ported memory is chosen from the group consisting of static random access memory and dynamic random access memory.

30. (Original) The integrated circuit of claim 27, wherein the multi-ported memory stores reservation bits mapped to blocks of general-purpose memory in the multi-ported memory.

31. (Previously Cancelled)

32. (Previously Cancelled

33. (Previously Cancelled)

Attorney's Docket No.:10559-364001/
Intel P8247-2

DRAFT

REMARKS

Claims 1-30 are pending in the application.

Claims 1-30 stand rejected under 35 U.S.C. 112, first paragraph.

Claims 1-6 and 9-29 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 4,371,923 to Dinwiddie, Jr. et al. ("Dinwiddie").

Claims 7-8 and 30 stand variously rejected under 35 U.S.C. 103 as allegedly being unpatentable over Dinwiddie in view of U.S. Patent No. 5,784,699 to McMahon et al. ("McMahon"), and U.S. Patent No. 5,546,554 to Young et al. ("Young,").

In view of the following remarks, Applicant respectfully traverses the rejections and asks that they be withdrawn. Reconsideration and allowance are respectfully requested.

I. The Rejections Under 35 U.S.C. 112

The office action alleges that claims 1-30 do not satisfy the written description requirement of 35 U.S.C. 112, first paragraph.

The Federal Circuit has made clear that the specification need not include verbatim support for claim terms. See, e.g. Purdue Pharma v. Faulding Corp., 230 F.3d 1320, 1324 (Fed. Cir. 2000). Rather, all that is needed to satisfy the written description requirement of 35 USC 112, first paragraph, is

DRAFT

disclosure in the application that reasonably conveys to an artisan that the inventor had possession at the time of filing of the claimed subject matter. See, e.g., In re Kaslow, 217 USPQ 1089 (Fed. Cir. 1983). The supporting disclosure need not be express but rather can be inherent. See, e.g., Atmel v. Information Storage Devices, 198 F.3d 1375, 1380 (Fed. Cir. 1999).

Here, the specification as filed includes several passages that reasonably convey to an artisan that applicants had in their possession at the time of filing the claimed subject matter.

Support for the feature that "the computer system is configured so that control accesses from the central processing unit are directed to the multi-ported memory and not to the main memory and data accesses from the central processing unit are directed to the main memory and not to the dual-ported memory" may be found, for example, on page 4, lines 3-5 of the current specification: "Computer architecture 10 offers a more efficient use of resources by directing control/status accesses to dual-ported memory 18 in controller 16, rather than to main memory 22." This portion clearly describes directing control accesses to the dual ported memory and not to ("rather than") the main memory.

DRAFT

Support for the feature that memory accesses are directed to the main memory and not to the dual-ported memory is found on page 8, lines 5-7, which states that "Memory controller's dual-ported memory 52 need not be restricted to reading or writing control/status accesses. In some circumstances, data may be stored in memory 52." A person skilled in the art would understand this portion to describe two situations: one in which data may be stored in memory 52 (i.e., data accesses may be directed to the multi-ported memory), and one in which the multi-ported memory is restricted to reading or writing control/status accesses (i.e., data accesses are directed to the main memory and not to the multi-ported memory). Both situations are clearly contemplated by the current specification.

Therefore, a person skilled in the art would understand that applicants had in their possession at the time of filing the claimed subject matter. Thus, claims 1-30 satisfy the written description requirement of 35 U.S.C. 112.

II. The Rejections Under 35 U.S.C. 102(b)

Claim 1

Claim 1 is patentable over Dinwiddie because Dinwiddie neither teaches nor suggests that control accesses from the central processing unit are "directed to the multi-ported memory

DRAFT

and not to the main memory," while data accesses from the central processing unit are "directed to the main memory and not to the multi-ported memory."

The office action asserts that column 5, lines 9-10 and 48-49 of Dinwiddie teaches that data accesses from the CPU are directed to the main memory and not to the dual-ported memory. (Please see page 3 of the office action). Since these passages discuss accesses to the dual port random access storage mechanism 22, the office action is clearly equating mechanism 22 with the main memory rather than the multi-ported memory.

Since the office action identifies mechanism 22 as the main memory of claim 1, control accesses would need to be directed to the multi-ported memory (equated with elements 25, 27, and 30 of Figure 1 in the office action), and not to mechanism 22.

However, Dinwiddie teaches that "Data passing from the channel bus 8 to the microprocessor bus 16 or vice versa is at least temporarily stored in this storage mechanism." (See column 4, lines 63-66 of Dinwiddie). Dinwiddie defines the term "data" in column 3, lines 47-51 as "Unless otherwise indicated by the context, the term 'Data' is used herein in its broadest sense as including any kind of information such as alphanumeric data, status information, control information, address values, and the like." Thus, dual port random access storage mechanism

DRAFT

22 performs the function of (at least temporarily) storing all data (data and status information) being transferred between the peripherals and the CPU. This proposition is stated even more clearly in the Abstract of Dinwiddie: "All data transfers are by way of the dual port storage unit."

Other portions of Dinwiddie support the interpretation that both data and control/status information is stored in mechanism 22. For example, column 11, line 66 to column 12, line 9 of Dinwiddie teaches that for a direct program control operation (DPC): "each DPC read type command enables a 2-byte word of data or status information to be transferred from the I/O controller 2 to the host processor 1. Each DPC write type operation enables a 2-byte word of data or control information to be transferred from the host processor 1 to the I/O controller 2. The DPC data word (IDCB bits 16-31) is transferred by way of the channel data bus 34 and is stored into or transferred out of the dual port storage unit 22a, 22b, with the higher order byte (Byte 2 or bits 16-23) being stored into or read from the high byte storage unit 22a and the lower order byte (Byte 3 or bits 24-31) being stored in or read from the low byte storage unit 22b." Thus, Dinwiddie teaches that both status and data accesses are directed to mechanism 22.

DRAFT

As noted in a previous reply, it appears that any modification of Dinwiddie to direct control and data accesses differently would render Dinwiddie unsatisfactory for its intended purpose. When a proposed modification would render the prior art invention being modified unsatisfactory for the intended purpose, then there is no suggestion or motivation to make the proposed modification (see MPEP 2143.01). If Dinwiddie were modified so that only data accesses were directed to mechanism 22, it would no longer function as a data transfer interface between the microprocessor bus and the host processor channel bus for all data. Since Dinwiddie describes this data transfer interface as "A primary feature of the new and improved I/O controller 2," (see column 4, lines 59-60 of Dinwiddie), there is no motivation to modify Dinwiddie so that control accesses are no longer directed to mechanism 22.

For at least the above reasons, claim 1 is patentable over Dinwiddie.

Claims 10, 14, 19, 23, and 27

Independent claims 10, 14, 19, 23, and 27 include features similar to those in claim 1, and are therefore patentable for at least the same reasons as stated above with respect to claim 1.

Attorney's Docket No.:10559-364001/
Intel P8247-2

DRAFT

Claims 2-9, 11-13, 15-18, 20-22, 24-26, and 28-30

Claims 2-9, 11-13, 15-18, 20-22, 24-26, and 28-30 depend from the independent claims noted above, and are therefore patentable for at least the same reasons.

Applicant believes that claims 1-30 are in condition for allowance and asks that all claims be allowed. Enclosed is a **Enter $ amount** check for excess claim fees and a **Enter $ amount** check for the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date:_____

_____
Scott C. Harris
Reg. No. 32,030
Attorneys for Intel Corporation

Fish & Richardson P.C.
Customer Number: 20985
4350 La Jolla Village Drive, Suite 500
San Diego, CA 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10263096.doc